## Fault Modeling, Fault Tolerance, and Test

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## Abstract

Fault diagnosis of ICs is essential to reduce design iterations in order to meet the time-to-market goal of the first prototypes. The paper takes a fresh look at lessons learned and where things stand today, along with prospects for a next future.

Keywords: MOS, VLSI, fault models and model faults, fault diagnosis, testing strategy

## **References:**

[1] International Technology Roadmap for Semiconductors, 2011 Edition, Test and Test Equipment, www.itrs.net/Links/2011itrs/.../2011Test.pdf.

[2] M. E. Zaghloul, "Physical Fault Modeling and Simulation for VLSI MOS Circuits", in Zobrist, G. W. (Ed.), VLSI Fault Modeling and Testing Techniques, Ablex Publishing Corp., Norwood, 1993.
[3] Belgacem Hamdi, Etienne Sicard, "Introduction to Fault Analysis at Logic Level – An Educational Approach Based on DSCH", www.mes.tu-darmstadt.de/...3/.../hamdi paper.pdf.

[4] K. N. Patel, et al., "Evaluating Circuit Reliability Under Probabilistic Gate-Level Fault Models," megaknowledge.info/cadathlon/.../p3-synthesis.pdf.

[5] Pradipkumar Arunbhai Thaker, Register-Transfer Level Fault Modeling and Test Evaluation Technique for VLSI Circuits, Ph. D. Thesis, George Washington University, 2000.

[6] Nor Zaidi bin Haron, Testability and Fault Tolerance for Emerging Nanoelectronic Memories, Ph. D. Thesis, Delft University, 2012.

[7] Chia Yee Ooi, Hideo Fujiwara, "Enhanced Functional Fault Model for Micro Operation Faults", isw3.naist.jp/IS/TechReport/report/2010004.pdf.

[8] Pradipkumar Arunbhai Thaker, Register-Transfer Level Fault Modeling and Test Evaluation Technique for VLSI Circuits, Ph. D. Thesis, George Washington University, 2000.

[9] Emmanuel Simeu, Salvador Mir, Libor Rufer, "Online Testing Embedded Systems: Adapting Automatic Control Techniques to Microelectronics Testing", http://www.nt.ntnu.no/users/skoge/prost/proceedings/ifac2005/Fullpapers/03994.pdf.