Systems on Chip (SoCs) and Reliability: Challenging Issues

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Abstract

SoCs and microelectromechanical systems (MEMS) technologies could possibly enable in the next few years various space mission applications, medical imaging, remote sensing field, computer and IR vision, or other image processing applications. This paper is intended to inform non-SoC and non-MEMS technologists, researchers, and decision makers not only about the rich potential applications, but also too about some not yet solved important reliability key problems of reconfigurable SoCs. We still have limited knowledge on how such devices fail. Biggest challenge: cost effective, high volume packaging, self-healing SoCs.

Keywords: SoCs, MEMS, CMOS technology, embedded systems, reliability, failure mechanisms

References:

[1] Simunic, T., K. Mihic, and G. De Micheli, "Optimization of Reliability and Power Consumption in Systems on a Chip," Integrated Circuit and System Design, 2005, pp. 237-246.

[2] Băjenescu, T., M. Bâzu, Reliability of Electronic Components. A Practical Guide to Electronic Systems Manufacturing, Springer, Berlin and New York, 1999.

[3] Vassighi, A., "Heat and Power Management for High Performance Integrated Circuits," Doctor of Philosophy Thesis Presented to the University of Waterloo, Ontario, Canada, 2004.

[4] Bernauer, A., et al., "An Architecture for Runtime Evaluation of SoC Reliability," http://www.ti.unituebingen.de/uploads/tx_timitarbeiter/bernauer-architecture-runtime-evaluation-soc-reliability-GIOC-06_01.pdf.

[5] Borkar, Shekhar, "Designing Reliable Systems From Unreliable Components: The Challenges of Transistor Variability and Degradation," IEEE Micro, 25(6), November/December 2005, pp. 10-16.

[6] Nourani, M., and A. R. Attarha, "Detecting Signal-Overshoots for Reliability Analysis in High-Speed System-on-Chips," IEEE Transactions on Reliability, Volume 51, Issue 4, Dec 2002, pp. 494-504.

[7] White Paper 2007, Virtuoso Ultrasim Full-Chip simulator, netlist-based electromigration voltage drop (EMIR) flow. http://www.cadence.com/rl/Resources/white_papers/emir_wp.pdf.

[8] ECSI Institute Workshop on Reconfigurable Systems-on-Chip, January 18, 2007, Hotel Ibis/Gares CDG Airport – Paris.

[9] Dallavalle, C., "Adaptive IDDQ: How to Set an IDDQ Limit for Any Device Under Test," Proceedings of the Eighth IEEE International On-Line Testing Workshop, 2002, p. 177.

[10] Chih-Wen Lu, Su Chauchin; Lee Chung Len, and Chen Jwu-E., "Is IDDQ Testing Not Applicable for Deep Submicron VLSI in Year 2011?," Proc. of the Ninth Asian Test Symposium, 2000. (ATS 2000), pp. 338-343.

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[11] Ackerman, R., "Doing More With Less: A Recipe for Rapid IDDQ Development," Proceedings of IEEE International Workshop on Current and Defect Based Testing, DBT, 2004, pp. 33-42.
[12] Masato Nakanishi, H. Masaki, H. Yotsuyanagi, M. Yukiya, "A BIC Sensor Capable of Adjusting IDDQ Limit in Tests," 15th Asian Test Symposium, ATS '06, 2006, November 2006, pp. 69-74.