SOFT-ERROR TOLERANCE FOR SUBMICRON CIRCUITS

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Abstract: *Drastic device shrinking, power supply reduction, and increasing operating speeds that accompany the technological evolution to deeper submicron, reduce significantly the noise margins and thus the reliability of deep submicron ICs. A more significant problem is related to the single-event upsets (SEUs). It is predicted that neutrons produced by the sun activity will affect dramatically the operation of future* **I***ntegrated* **C***ircuits (***Ic***s). Self-test and fault tolerance in submicron and nanotechnologies becoming hitherto imperative. Perhaps the most significant problem concerns the sensitivity of future IC generations face to various noise sources, and in particularly face to energetic particles. In this context, this paper analyses some of problems related to the design of soft-error tolerant circuits*

Keywords: *fault tolerance, soft error, error detection, error masking, redundancy.*